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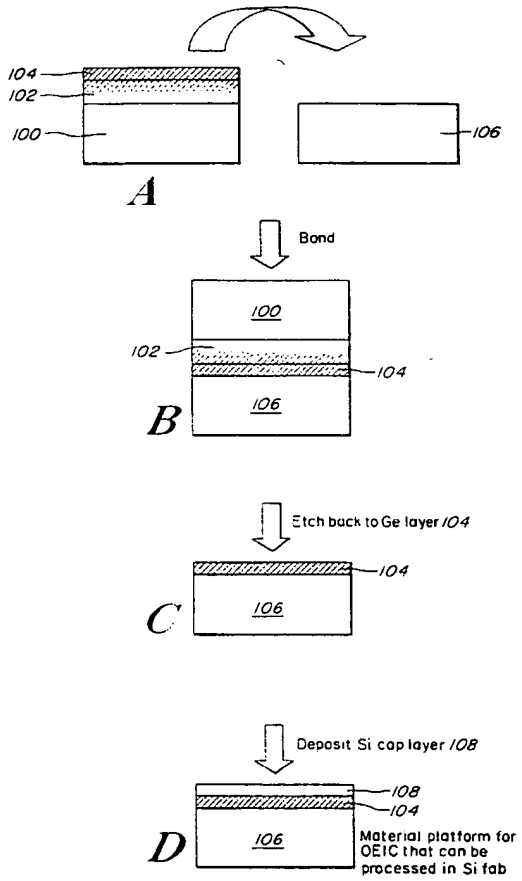
(54) Title: SILICON WAFER WITH EMBEDDED OPTOELECTRONIC MATERIAL FOR MONOLITHIC OEIC




(57) Abstract: A structure with an optically active layer embedded in a Si wafer, such that the outermost epitaxial layer exposed to the CMOS processing equipment is always Si or another CMOS-compatible material such as $SiO_2$. Since the optoelectronic layer is completely surrounded by Si, the wafer is fully compatible with standard Si CMOS manufacturing. For wavelengths of light longer than the bandgap of Si (1.1 μm), Si is completely transparent and therefore optical signals can be transmitted between the embedded optoelectronic layer and an external waveguide using either normal incidence (through the Si substrate or top Si cap layer) or in-plane incidence (edge coupling).

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# SILICON WAFER WITH EMBEDDED OPTOELECTRONIC MATERIAL FOR MONOLITHIC OEIC

## PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/223,407 filed August 4, 2000.

## BACKGROUND OF THE INVENTION

The invention relates to an epitaxial structure that contains optoelectronic material or semiconductor devices embedded in Si, such that the entire wafer can be processed using traditional Si CMOS tools to create a true monolithic optoelectronic integrated circuit (OEIC). The invention also relates to a monolithic optoelectronic integrated circuit (OEIC) formed on a Si substrate, based on optically-active semiconductor material embedded in a Si wafer such that the entire wafer can be processed using traditional Si CMOS tools to create the OEIC.

It has been a long-standing desire of the microelectronics and telecommunications industries to combine optoelectronic components with Si circuitry. Adding optoelectronic functionality to standard Si integrated circuits (ICs) would enable a tremendous range of new applications and devices, such as on-chip optical communication (enabling optical clock timing for high speed processors), inter-chip optical communication links (optical interconnects), and more efficient and compact optical transceivers for data communications and telecommunications.

Although hybrid integration of optical components with Si ICs provides a possible solution, this is not the preferred solution. True monolithic integration of optoelectronics with Si circuitry is far superior to hybrid integration for several reasons. Monolithic integration yields more compact devices (and therefore higher device integration densities); lower packaging costs since wire bonds or flip-chip bonds between the optoelectronic component and Si IC necessary in hybrid integration schemes are eliminated; lower processing costs since the entire device can be processed using standard Si CMOS techniques; and improved device characteristics in applications where hybrid integration yields undesirable electrical parasitics.

It is therefore desirable to create a truly monolithic structure containing both

optoelectronic functionality and Si CMOS circuitry. However, an intrinsic problem with integrating optoelectronic functionality into Si chips is that Si itself is not a good optoelectronic material as it neither emits nor detects light efficiently. Therefore, the optically active material integrated with the Si CMOS circuitry must be something other than Si, such as Ge, SiGe, GaAs, InP, AlGaAs, InGaAs, InGaAsP, or any other optically active group IV or III-V semiconductor material. Due to the large lattice mismatch and thermal expansion coefficient mismatch between these materials and Si, monolithically integrated devices created until now have been performance limited by the resulting crystalline defects (specifically threading dislocations) from epitaxy. However, recent progress in defect filtering schemes, such as graded buffer layers or selective epitaxial growth and epitaxial lateral overgrowth, has overcome this problem and enabled the creation of lattice-mismatched epitaxial layers of suitable quality for optoelectronic devices, such as photodetectors, light emitting diodes (LEDs), and lasers.

A major limitation of monolithic optoelectronic integrated circuits created until now has been the requirement that all Si CMOS processing steps be fully completed before integration of the optically active material. This requirement has existed because Si CMOS processing tools cannot be exposed to any other materials due to contamination concerns.

## SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide an epitaxial structure in which an optically active material or semiconductor devices are embedded within Si such that the entire wafer can be processed using traditional Si CMOS tools to yield a true monolithic optoelectronic integrated circuit. It is also an object of the invention to provide a method by which such a wafer structure may be obtained.

The invention provides a structure in which the optically active layer is embedded in a Si wafer, such that the outermost epitaxial layer exposed to the CMOS processing equipment is always Si (or another CMOS-compatible material such as $SiO_2$). Since the optoelectronic layer is completely surrounded by Si, the wafer is fully compatible with standard Si CMOS manufacturing. Therefore, all of the manufacturing and cost benefits associated with Si CMOS processing are fully realized by the invention.

It is important to note that embedding the optoelectronic layer in Si does not prevent transmission of optical signals between the OEIC and an external waveguide (such as an optical fiber) or free space. Specifically, for wavelengths of light longer than the bandgap of Si (1.1 μm), Si is completely transparent and therefore optical signals can be transmitted between the embedded optoelectronic layer and an external waveguide using either normal incidence (through the Si substrate or top Si cap layer) or in-plane incidence (edge coupling). This provides tremendous flexibility in designing an OEIC used for the typical telecommunications wavelengths of 1.3 and 1.55 μm. Additionally, even wavelengths shorter than the bandgap of Si can be coupled in and out of the embedded optoelectronic layer. This is because the top Si cap layer can be made thin enough that it is only minimally absorbing at other commonly used wavelengths, such as 980 or 850 nm. Alternatively, edge coupling could be used for these wavelengths. This flexibility facilitates design of complex system-on-a-chip structures where multiple wavelengths and/or multiple optical in/out connections are required.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-1D are block diagrams of an exemplary embodiment of a graded buffer/wafer bonding process to create an optically-active layer embedded in a Si wafer in accordance with the invention;

Figs. 2A-2D are block diagrams of another exemplary embodiment of a graded buffer/wafer bonding process to create a more complex wafer structure that contains an insulating layer between the optically-active layer and the Si substrate;

Figs. 3A-3D are block diagrams of yet another exemplary embodiment of a graded buffer/wafer bonding process to create a yet more complex wafer structure that contains a Si contact layer between the insulating layer and optically-active layer;

Figs. 4 are block diagrams showing the resulting wafer structure of still yet another exemplary embodiment of a graded buffer/wafer bonding process, wherein the optically-active layer is isolated from both the Si substrate and the Si cap layer by insulating layers, and showing a possible implementation of the Si CMOS electronics to create a monolithic optoelectronic integrated circuit;

Figs. 5A-5C are block diagrams of an exemplary embodiment of a graded buffer/wafer bonding process where the original substrate and graded buffer layer are not removed from the structure;

Figs. 6A-6C are block diagrams showing an exemplary embodiment of an OEIC processing such that the Si CMOS electronics are located in the Si substrate below the optically-active layer; and

Figs. 7 is a block diagram of an exemplary embodiment of an OEIC implementation in which emitters, detectors, and Si CMOS electronics have all been monolithically integrated on the same Si substrate.

## DETAILED DESCRIPTION OF THE INVENTION

There are several different techniques available to monolithically integrate lattice-mismatched materials, including wafer bonding, graded buffer layers, and epitaxial lateral overgrowth. Wafer bonding is an attractive option because it can directly combine two dissimilar materials together without the need for an "interlayer structure", e.g., a graded buffer layer or selective epitaxial mask. However, even though wafer bonding eliminates the lattice-mismatch problem, two new problems arise which have prevented wafer bonding from reaching its full potential: thermal expansion mismatch and wafer size mismatch.

Thermal expansion mismatch is a serious issue when the dissimilar wafers being bonded are of similar thickness. This mismatch can cause large strains to develop during heating and cooling that can crack the assembly or cause the wafers to debond. Wafer size mismatch relates to the fact that two dissimilar wafers being bonded typically have different diameters. Therefore, some fraction of the larger diameter wafer is wasted. For example, consider bonding a Si substrate and a Ge substrate. Si substrates are commonly available in an eight-inch diameter, while Ge is commonly available only four inches in diameter. Therefore, only a portion of the Si substrate would be covered by the bonding process, while the rest of the wafer would be wasted.

The combination of graded layer growth and wafer bonding removes these two problems and provides tremendous flexibility to create new integrated semiconductor platforms on Si substrates. Consider again the example of bonding Ge to Si, this time using the graded layer/wafer bonding technique illustrated in Figs. 1A-1D. In this

technique, a graded SiGe layer 102 (graded from 0-100% Ge) is epitaxially grown on a Si substrate 100 of any diameter. A Ge layer 104 is then grown on the SiGe graded layer 102. In order to reduce surface roughness, a planarization step such as chemical mechanical polishing can be inserted during growth of the SiGe graded layer 102, as described in U.S. Pat. No. 6,107,653, incorporated herein by reference. Also note that any of the layers described in this invention can receive planarization steps, if desired.

The wafer can then be bonded to another Si substrate 106, of the same diameter as shown in Figs. 1A and 1B. This technique therefore eliminates the wafer size mismatch issue, and it also eliminates the thermal mismatch issue because both wafers are essentially Si.

Once the wafers are bonded, the original Si substrate 100 can then be ground and selectively etched back. In one embodiment (shown in Fig. 1C), the SiGe graded layer 102 can also be completely removed to leave only the Ge layer 104 on the new host Si substrate 106. A Si cap layer 108 can now be epitaxially grown on top of this structure, such that the optically-active layer 104 (Ge in this case) is effectively embedded in a Si wafer as shown in Fig. 1D.

Although the large lattice mismatch (about 4%) between Ge and Si will create many dislocations during this final Si deposition, they will only reside in the Si cap layer 108, and will not penetrate into the optoelectronic Ge layer 104. This is because for systems with a large lattice mismatch (typically greater than 1.5%) the growth mode is such that dislocations can only achieve short glide distances and therefore will remain in the deposited film. Penetration of misfit dislocations into the underlying film layer (Ge in this case) requires long dislocation glide distances typically only achieved for systems with a lattice mismatch $<1.5\%$. These dislocations in the Si cap layer 108 will not have a deleterious effect on device operation if the CMOS electronics are located in the Si substrate 106 (see Figs. 6A-6C), rather than in the Si cap layer 108.

In another embodiment, a Si cap layer could be wafer bonded (from another Si substrate) on top of the optically active layer, rather than epitaxially grown. In this embodiment, the Si cap layer would be of high quality, and therefore could be processed into CMOS circuits containing field effect transistors (FETs) or similar devices. In yet another embodiment, the original SiGe graded layer 102 could be only partially removed during etch back, such that a strained Si cap layer could be

epitaxially grown on top of the remaining SiGe graded layer 102. This strained Si cap layer would be of high quality, and could be processed into CMOS circuits with enhanced performance compared to relaxed Si CMOS circuits. In still yet another embodiment, the original Si substrate 100 and SiGe graded layer 102 could be completely removed, and a uniform composition SiGe layer could be wafer bonded on top of the optically active layer. A strained Si cap layer could then be epitaxially grown on this SiGe layer and could be processed into CMOS circuits.

It will be appreciated by those skilled in the art that techniques other than grinding/etch back, such as delamination, can be used to remove the Si substrate 100 and graded SiGe layer 102 from the first wafer.

It will also be appreciated by those skilled in the art that additional layers could potentially be incorporated into the structure. For example, in another embodiment as illustrated in Figs. 2A-2D, a first Si substrate 200 can have a 0-100% graded SiGe layer 202 with a Ge layer 204 on top as before, while a second Si substrate 206 can have a thick insulating layer 208 on its surface, such as $SiO_2$. This insulating layer will serve to isolate the optoelectronic layer 204 from the Si substrate 206 (and any CMOS electronics subsequently processed in said substrate). A (highly defective) Si layer 210 can again be deposited on top of the optoelectronic layer 204.

In yet another embodiment as illustrated in Figs. 3A-3D, after a graded SiGe 300 and Ge layers 302 are grown on a first Si substrate 304, a Si cap layer 306 can be grown on the Ge layer 302. An optional $SiO_2$ layer can then be grown or deposited on this Si cap layer to aid in wafer bonding. Although this Si cap layer 306 will have a high density of dislocations, they will not deleteriously affect device performance since this Si layer 306 will not be active optically or electronically. One benefit of including this Si cap layer 306 in the heterostructure is to serve as an etch stop when forming the bottom contact to the Ge layer 302. This wafer can then be bonded to another Si substrate 308 which has an insulating layer 310, such as $SiO_2$, on it as before. After etching back to the Ge layer 302, another Si cap layer 312 can be provided.

In still yet another embodiment as illustrated in Figs. 4A-4B, an insulating layer 400 can be inserted between a top Si cap layer 402 and an optically active layer 404. This would be useful to isolate the optically-active layer 404 from the CMOS electronics in a particular OEIC embodiment where the CMOS electronics were located in the top Si cap layer 402, rather than in the Si substrate 408.

As shown in Figs. 5A-5C, it is also possible to have an embodiment in which an original Si substrate 500 is not removed. One such structure would involve growing a graded SiGe layer (graded 0-100%) 502, and then a uniform Ge layer 504 as the optically active layer. A second Si substrate 506 with a $SiO_2$ layer 508 can then be wafer bonded on top of the Ge layer 504. The second Si substrate 506 can then be partially etched-back or delaminated to leave a thin Si cap layer 510, which is substantially defect-free. The CMOS electronics would be processed into a top Si cap layer 510 in this embodiment. Additional layers could also be included in this embodiment as discussed above, such as a relaxed SiGe layer with a strained Si cap layer for strained Si CMOS.

It is to be understood that additional layers that serve various purposes could be included in the structure. For example, layers could be included at various heterointerfaces to minimize the (possibly deleterious) effect of energy band discontinuities at these heterointerfaces. As another example, quarter-wavelength-thick layers of materials of alternating high- and low-refractive index could be grown or deposited on top of either wafer before bonding such that a high-reflectance multilayer stack would exist below the optoelectronic material. This stack could serve as the lower mirror of a resonant cavity to enhance optical responsivity at a particular wavelength. During subsequent processing of the bonded wafers, a high-reflectance mirror could be deposited above the optoelectronic layer to complete the resonant cavity, or the uppermost ambient/semiconductor interface could serve as the top mirror.

The structures and techniques described are extendable to other optoelectronic materials besides Ge. For example, simply by grading the SiGe graded layer on the first Si substrate to a certain composition less than 100% Ge, and then growing a uniform layer of SiGe at that composition, a SiGe layer of that composition could be embedded in a Si wafer as the optically-active layer.

As another example, through compositional grading of SiGe and InGaAs layers on Si, it is possible to create a bonded layer of InP or InGaAs on Si as well. This can be accomplished as follows. First, a graded SiGe epitaxial layer (graded from 0-100% Ge) is epitaxially grown on a Si substrate. Since GaAs and Ge have nearly equal lattice constants, a GaAs layer can then be epitaxially grown on top of the Ge layer. At this point, the GaAs layer can be wafer bonded to another Si substrate such that the

embedded active optoelectronic layer was GaAs. Alternatively, a relaxed, graded InGaAs layer can be grown on the GaAs layer, graded from 0% In to some desired In concentration, as described in U.S. Pat. No. 6,232,138, incorporated herein by reference. The InGaAs layer can be wafer bonded to another Si substrate.

In yet another embodiment, InGaAsP or InP lattice-matched to $In_{0.53}Ga_{0.47}As$ can be grown on the structure and wafer bonded to another Si substrate. In yet a more complicated embodiment, lattice-matched heterostructures for various optoelectronic devices can be epitaxially grown on the first wafer, and wafer bonded to the second Si substrate.

As an example, a relaxed SiGe graded layer can be grown from 0-100% Ge on the first Si substrate, on top of which a relaxed, graded InGaAs layer can then be grown from 0-53% In. A lattice-matched InP layer could then be grown, and serve as the starting substrate for any optoelectronic device lattice-matched to InP. For example, a laser structure containing InP, InGaAs, and InGaAsP, all lattice-matched to InP, can then be grown. The entire device structure can be wafer bonded to a second Si substrate, such that the embedded optoelectronic layer in this case was an entire laser (or LED or detector) structure, rather than a single layer as described with Ge. Of course, the structure would have to be grown "upside-down" on the original Si substrate since it would be inverted upon being wafer bonded to the second Si substrate. Similarly, an entire heterostructure lattice-matched to GaAs could be grown on the first Si substrate and then wafer bonded to the second Si substrate.

These other optoelectronic layers can also be coated with Si, such that the embedded optically-active semiconductor material can be chosen from a wide range of materials, including: Ge, SiGe, GaAs, AlGaAs, InGaAs, InP, InGaAsP, any III-V alloy lattice-matched to GaAs, any III-V alloy lattice-matched to InP, any multiple-layer heterostructure (a laser, light emitting diode, or photodetector) lattice-matched to GaAs, or any multiple-layer heterostructure lattice-matched to InP.

Once the planar composite wafer has been fabricated, it contains at a minimum a Si substrate, a layer of optically active material, and a Si cap layer. It may also include optional additional layers or device heterostructures as described. This structure can be processed to create a monolithic optoelectronic integrated circuit. For example, consider the case of creating an optical receiver circuit on Si. The optical receiver could contain a detector and receiver circuit, or multiple detectors and a

receiver circuit(s). Since the optically active layer is completely embedded in a Si wafer, this planar composite wafer can be processed as a normal Si wafer would be for CMOS manufacturing.

In one embodiment as illustrated in Figs. 6A-6C, a starting wafer heterostructure 600 based on the resulting structure shown in Fig. 3D, Si CMOS electronics 602 can be processed on the Si substrate. In this embodiment, an early step would include patterning the wafer to define the optoelectronic receiver areas, and these areas would be protected with a mask. The other areas would be etched down to the Si substrate, leaving a virgin Si surface to be processed into CMOS electronics.

It is expected that special attention may be required for the CMOS processing thermal budget to minimize the interdiffusion of (and maintain the integrity of) the embedded optoelectronic layer. However, the thermal budget and controlled interdiffusion could also be used to the device designer's advantage. For example, a slight interdiffusion at the upper and lower surfaces of the optically-active layer (Ge in this example) would grade these interfaces and therefore minimize sharp energy band discontinuities that might be deleterious for certain devices. After CMOS processing is complete, the areas with Ge can then be processed into detectors, and final interconnections can be made between the Si CMOS circuit and the Ge detectors.

Alternatively, in another embodiment shown in Fig. 4D, the Si CMOS electronics can also be fabricated above the optoelectronic layer, rather than co-planar with it. Rather than epitaxially growing a highly-defective Si cap layer above the optoelectronic (Ge in this example) layer, a high-quality Si cap layer can be wafer bonded above the optoelectronic layer as described. The Si CMOS electronics can be formed in this Si cap layer above the optoelectronic layer, rather than in the Si substrate. Vias can be drilled through this top Si CMOS layer to provide contacts to the underlying optoelectronic layer where desired. Underlying Si layers could serve as etch stops, as mentioned above. Individual components can be isolated from one another using trench isolation.

In yet another embodiment, the CMOS circuits can be fabricated in a strained Si cap layer above the optoelectronic layer as described, rather than in a relaxed Si cap layer. This can be achieved by wafer bonding (or epitaxially growing) a relaxed SiGe layer of a desired composition on top of the optoelectronic (Ge) layer. A strained Si cap layer can then be epitaxially grown on top of the relaxed SiGe layer. Again, vias

can be drilled through the strained Si and relaxed SiGe layers to contact the optoelectronic layer where desired.

The optoelectronic layer being embedded in Si has several advantages. First, the entire integration sequence can occur within a Si foundry. Even the interconnects between the Si CMOS and optoelectronic layer can be performed with Si contact technology, since the contact which will be formed in the optoelectronic region will be a contact to the Si cap layer on the optoelectronic layer. All contact and interconnect materials could be based on standard Si VLSI processing. For example, contacts could be made using Ni, Co, or Ti, and the resulting silicides. Via plugs can use tungsten, while metal interconnect lines can use Al or Cu. Also, the large defect density in the Si contact layers (present in certain embodiments) will aid in creating low resistance contacts, since these defects will enhance interdiffusion and diffusion.

Alternatively, since the Si layers are deposited epitaxially in some embodiments, the doping can be controlled with epitaxy and high thermal budgets for activating implants are not needed in these embodiments. Additionally, Ge-based optically active regions do not necessarily need to be doped during the epitaxial process. Since Ge is isoelectronic with Si, the same elements that dope Si will dope Ge. Thus, given the current process simulation tools, one can simply dope the Si contact layers (in certain embodiments where the Ge layer directly contacts a Si layer at its upper and lower surfaces, i.e. Fig. 3D) and leave the Ge intrinsic; during subsequent processing, the dopants can enter the Ge, creating the p-i-n structure in Ge needed for photodiode behavior. Also, in situ deposition of a Si layer on top of the Ge will help prevent the surface nucleation of cracks in the Ge due to the thermal expansion difference between Si and Ge.

Finally, it is important to note that since Si has a larger bandgap than the optical wavelengths of light typically used in telecommunications (1.3 and 1.55 μm), the Si substrate and top cap layer are both transparent to these wavelengths. Thus, transmission of optical signals between the embedded optoelectronic layer and an external waveguide (such as an optical fiber or free space) can easily occur by either normal incidence through the front or backside of the wafer, or in-plane incidence. Additionally, even wavelengths shorter than the bandgap of Si can be coupled in and out of the embedded optoelectronic layer. This is because the top Si cap layer can be made thin enough that it is only minimally absorbing at other commonly used

wavelengths, such as 980 or 850 nm. Alternatively, edge coupling could be used for these wavelengths.

Thus, the embedded optically-active layers can be used for the creation of complex integrated optoelectronic transceivers. One can therefore construct, for example, optical network switches on a chip. A schematic example of such an OEIC 700 is shown in Fig. 7. In this example, an InGaAs/InP heterostructure has been embedded in a Si wafer 702. Certain regions have been processed to form emitters 704 using this embedded optically-active material, while other regions have been processed to form detectors 706. The diagram has been drawn simplistically for clarity, as the InGaAs/InP emitters and detectors are not actually exposed on the surface of the wafer. They are embedded in the wafer 702. The top layer of the entire structure is Si.

A simple structure that would enable the formation of both emitters and detectors is a p-i-n structure, which would emit light when forward-biased, and detect light when reverse-biased. In another region of the wafer, Si electronics 708 have been processed into the Si substrate. The Si electronics are connected to the optoelectronic devices using interconnects based on standard Si interconnect materials, such as Al or Cu. Additionally, since the entire top surface of the wafer is a Si cap layer, the contacts to the optoelectronic emitters and detectors can be made using standard Si contact materials, such as Ni, Co, or Ti silicides. Finally, optical signals can be transmitted between the OEIC and external optical fibers. One possibility is shown in the figure, where the light is transmitted through the substrate to butt-coupled fibers 710. The optical signals could also be transmitted through the Si cap layer, such that optical fibers would be positioned above the OEIC. A third possibility is to use edge coupling, where v-grooves would be etched in the substrate to align optical fibers for in-plane incidence.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

## CLAIMS

1. A semiconductor heterostructure comprising:

a Si substrate;

an optically active semiconductor material on said substrate, said optically active semiconductor material being lattice mismatched with respect to said substrate and substantially relaxed; and

a cap layer on said optically active semiconductor material, said cap layer comprising Si.

2. The heterostructure of claim 1, wherein said optically active semiconductor material comprises material from the group of: Ge, GaAs, InP, AlGaAs, InGaAs, InGaAsN, InGaAsP, a III-V alloy lattice-matched to GaAs, or a III-V alloy lattice-matched to InP.

3. The heterostructure of claim 1, wherein said optically active semiconductor material comprises SiGe.

4. The heterostructure of claim 1, wherein said optically active semiconductor material comprises a multiple layer heterostructure lattice-matched to GaAs, or a multiple layer heterostructure lattice-matched to InP.

5. The heterostructure of claim 1, wherein said optically active semiconductor material has a smaller bandgap than the bandgap of Si.

6. The heterostructure of claim 1, wherein said cap layer is monocrystalline and substantially defect-free.

7. The heterostructure of claim 1, wherein said cap layer is monocrystalline and highly defective.

8. The heterostructure of claim 1 further comprising a relaxed, graded $Si_{1-x}Ge_x$ layer graded from $x=0$ to $x \leq 1$, positioned between said Si substrate and said optically active semiconductor material.

9. The heterostructure of claim 8 further comprising a relaxed, graded $In_xGa_{1-x}As$ layer graded from $x=0$ to $x\leq 1$, positioned between said relaxed, graded $Si_{1-x}Ge_x$ layer and said optically active semiconductor material.

10. The heterostructure of claim 1, wherein at least one layer has been planarized.

11. The heterostructure of claim 1 further comprising an insulating layer on said substrate, said optically active semiconductor material being positioned on said insulating layer.

12. The heterostructure of claim 1 further comprising an insulating layer on said optically-active semiconductor material, said cap layer being positioned on said insulating layer.

13. The heterostructure of claim 1 further comprising:

a first insulating layer on said substrate, said optically active semiconductor material being positioned on said first insulating layer; and

a second insulating layer on said optically active semiconductor material, said cap layer being positioned on said second insulating layer.

14. The heterostructure of claim 1 further comprising:

a first insulating layer on said substrate;

a first Si layer on said first insulating layer, said optically active semiconductor material being positioned on said first Si layer;

a second Si layer on said optically active semiconductor material; and

a second insulating layer on said second Si layer, said cap layer being positioned on said second insulating layer.

15. The heterostructure of claim 14, wherein said Si contact layers are monocrystalline and highly defective.

16. The heterostructure of claim 1, wherein said cap layer comprises a relaxed SiGe layer with a strained Si cap layer.

17. A method of fabricating a semiconductor heterostructure comprising:

providing an optically active semiconductor material on a substrate, said optically active semiconductor material being lattice mismatched with respect to said substrate and substantially relaxed; and

providing a cap layer on said optically active semiconductor material, said cap layer comprising Si.

18. The method of claim 17 further comprising providing a relaxed, graded $Si_{1-x}Ge_x$ layer graded from $x=0$ to $x\leq 1$, positioned between said Si substrate and said optically active semiconductor material.

19. The method of claim 18 further comprising providing a relaxed, graded $In_xGa_{1-x}As$ layer graded from $x=0$ to $x\leq 1$, positioned between said relaxed, graded $Si_{1-x}Ge_x$ layer and said optically active semiconductor material.

20. The method of claim 17 further comprising an insulating layer on said substrate, said optically active semiconductor material being positioned on said insulating layer.

21. The method of claim 17 further comprising providing an insulating layer on said optically active semiconductor material, said cap layer being positioned on said insulating layer.

22. The method of claim 17 further comprising:

providing a first insulating layer on said substrate, said optically active semiconductor material being positioned on said first insulating layer; and

providing a second insulating layer on said optically active semiconductor material, said cap layer being positioned on said second insulating layer.

23. The method of claim 17 further comprising:

providing a first insulating layer on said substrate;

providing a first Si layer on said first insulating layer, said optically active semiconductor material being positioned on said first Si layer;

providing a second Si layer on said optically active semiconductor material; and

providing a second insulating layer on said second Si layer, said cap layer being positioned on said second insulating layer.

24. The method of claim 17, wherein said cap layer comprises a relaxed SiGe layer with a strained Si cap layer.

25. A semiconductor heterostructure comprising:

a Si substrate;

an optically active semiconductor device on said substrate, said optically active semiconductor device comprising at least one layer lattice-mismatched with respect to said substrate and substantially relaxed; and

a cap layer on said optically active semiconductor device, said cap layer comprising Si.

26. The semiconductor heterostructure of claim 25, wherein said optically active semiconductor device comprises a laser or light emitting diode.

27. The semiconductor heterostructure of claim 25, wherein said optically active semiconductor device comprises a photodetector.

28. The semiconductor heterostructure of claim 25, wherein said optically active semiconductor device comprises an optical modulator.

29. The semiconductor heterostructure of claim 25, wherein said optically active semiconductor device comprises at least one material from the group of: Ge, GaAs, InP, AlGaAs, InGaAs, InGaAsN, InGaAsP, a III-V alloy lattice-matched to GaAs, or a III-V alloy lattice-matched to InP.

30. The semiconductor heterostructure of claim 25, wherein said optically active semiconductor device comprises SiGe.

31. The semiconductor heterostructure of claim 25, wherein said optically active semiconductor device comprises a multiple layer heterostructure lattice-matched to GaAs, or a multiple layer heterostructure lattice-matched to InP.

32. The semiconductor heterostructure of claim 25, wherein said optically active semiconductor device operates at a wavelength for which Si is transparent.

33. The semiconductor heterostructure of claim 25 further comprising a relaxed, graded $Si_{1-x}Ge_x$ layer graded from $x=0$ to $x\leq 1$, positioned between said Si

substrate and said optically-active semiconductor device.

34. The semiconductor heterostructure of claim 33 further comprising a relaxed, graded $In_xGa_{1-x}As$ layer graded from $x=0$ to $x\leq 1$, positioned between said relaxed, graded $Si_{1-x}Ge_x$ layer and said optically active semiconductor device.

35. The semiconductor heterostructure of claim 25, wherein at least one layer has been planarized.

36. The semiconductor heterostructure of claim 25 further comprising an insulating layer on said substrate, said optically active semiconductor device being positioned on said insulating layer.

37. The semiconductor heterostructure of claim 25 further comprising an insulating layer on said optically active semiconductor device, said cap layer being positioned on said insulating layer.

38. The semiconductor heterostructure of claim 25 further comprising:

a first insulating layer on said substrate, said optically active semiconductor device being positioned on said first insulating layer; and

a second insulating layer on said optically active semiconductor device, said cap layer being positioned on said second insulating layer.

39. The semiconductor heterostructure of claim 25 further comprising:

a first insulating layer on said substrate;

a first Si layer on said first insulating layer, said optically active semiconductor device being positioned on said first Si layer;

a second Si layer on said optically active semiconductor device; and

a second insulating layer on said second Si layer, said cap layer being positioned on said second insulating layer.

40. The semiconductor heterostructure of claim 25, wherein said cap layer comprises a relaxed SiGe layer with a strained Si layer on top.

41. An optoelectronic integrated circuit comprising:

a Si substrate;

at least one optically active semiconductor material on said substrate, said at least one optically active semiconductor material being lattice-mismatched to said substrate and substantially relaxed; and

a cap layer comprising a CMOS-processing-compatible material on said at least one optically active semiconductor material.

42. The optoelectronic integrated circuit of claim 41 further comprising at least one Si layer and/or at least one insulating layer positioned between said Si substrate and said at least one optically active semiconductor material, and/or positioned between said at least one optically active semiconductor material and said cap layer.

43. The optoelectronic integrated circuit of claim 42, wherein said at least one insulating layer comprises $SiO_2$.

44. The optoelectronic integrated circuit of claim 41, wherein said cap layer comprises substantially defect-free monocrystalline Si.

45. The optoelectronic integrated circuit of claim 41, wherein said cap layer comprises highly-defective monocrystalline Si.

46. The optoelectronic integrated circuit of claim 41, wherein said cap layer comprises $SiO_2$.

47. The optoelectronic integrated circuit of claim 41, wherein said cap layer comprises substantially relaxed SiGe, and a strained Si cap layer on said substantially relaxed SiGe.

48. The optoelectronic integrated circuit of claim 41, wherein said at least one optically active semiconductor material comprises at least one material from the group of: Ge, GaAs, InP, AlGaAs, InGaAs, InGaAsN, InGaAsP, a III-V alloy lattice-matched to GaAs, or a III-V alloy lattice-matched to InP.

49. The optoelectronic integrated circuit of claim 41, wherein said at least one optically active semiconductor material comprises SiGe.

50. The optoelectronic integrated circuit of claim 41, wherein said at least one optically active semiconductor material comprises a multiple layer heterostructure

lattice-matched to GaAs, or a multiple layer heterostructure lattice-matched to InP.

51. The optoelectronic integrated circuit of claim 41, wherein said at least one optically active semiconductor material comprises a material for which Si is transparent.

52. The optoelectronic integrated circuit of claim 44 formed by first removing said substantially defect-free monocrystalline Si cap layer and said at least one optically active semiconductor material from a region of the Si wafer to expose said Si substrate; processing said exposed regions to form at least one Si device; processing said at least one optically active semiconductor material in remaining regions to form at least one optically active semiconductor device; and connecting said at least one Si device to said at least one optically active semiconductor device using at least one interconnect.

53. The optoelectronic integrated circuit of claim 44 formed by processing said substantially defect-free monocrystalline Si cap layer to form at least one Si device; processing said at least one optically active semiconductor material to form at least one optically active semiconductor device; and connecting said at least one Si device to said at least one optically active semiconductor device using at least one via.

54. The optoelectronic integrated circuit of claim 45 formed by first removing said highly-defective monocrystalline Si cap layer and said at least one optically active semiconductor material from a region of the Si wafer to expose said Si substrate; processing said exposed regions to form at least one Si device; processing said at least one optically active semiconductor material in remaining regions to form at least one optically-active semiconductor device; and connecting said at least one Si device to said at least one optically active semiconductor device using at least one interconnect.

55. The optoelectronic integrated circuit of claim 46 formed by first removing said $SiO_2$ cap layer and said at least one optically active semiconductor material from a region of the Si wafer to expose said Si substrate; processing said exposed regions to form at least one Si device; processing said at least one optically active semiconductor material in remaining regions to form at least one optically active semiconductor device; and connecting said at least one Si device to said at least one optically active semiconductor device using at least one interconnect.

56. The optoelectronic integrated circuit of claim 47 formed by processing said strained Si cap layer to form at least one Si device; processing said at least one optically active semiconductor material to form at least one optically active semiconductor device; and connecting said at least one Si device to said at least one optically active semiconductor device using at least one via.

57. The optoelectronic integrated circuit of claim 1 formed by first removing said cap layer and said at least one optically active semiconductor material to expose regions of said Si substrate; processing said exposed regions to form at least one Si device; processing said at least one optically active semiconductor material in remaining regions to form at least one optically active semiconductor device; and connecting said at least one Si device to said at least one optically active semiconductor device using at least one interconnect.

58. The optoelectronic integrated circuit of claim 1 formed by processing said cap layer to form at least one Si device; processing said at least one optically active semiconductor material to form at least one optically active semiconductor device; and connecting said at least one Si device to said at least one optically active semiconductor device using at least one via.

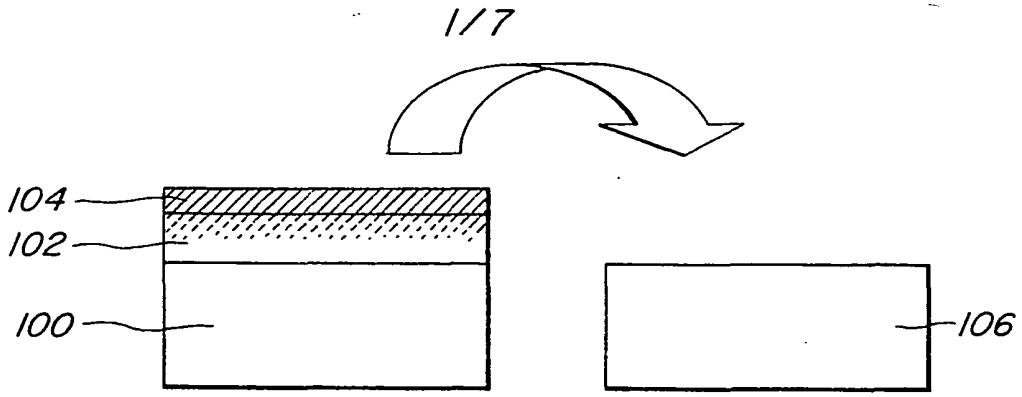


FIG. 1A

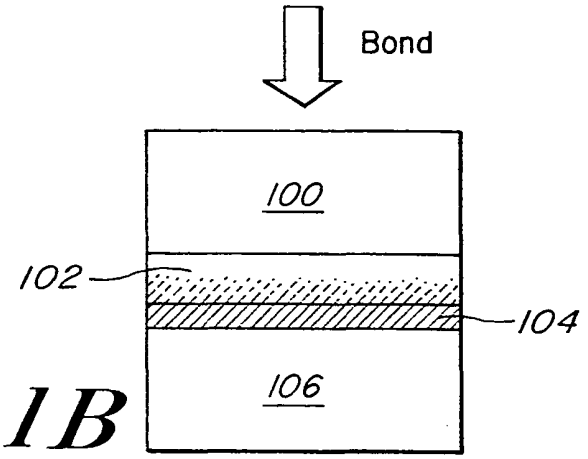


FIG. 1B

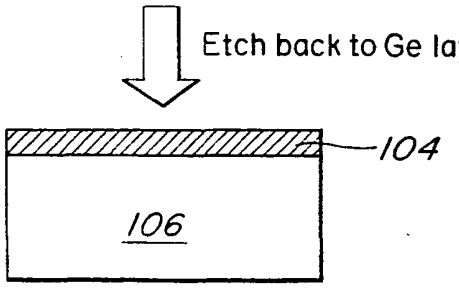


FIG. 1C

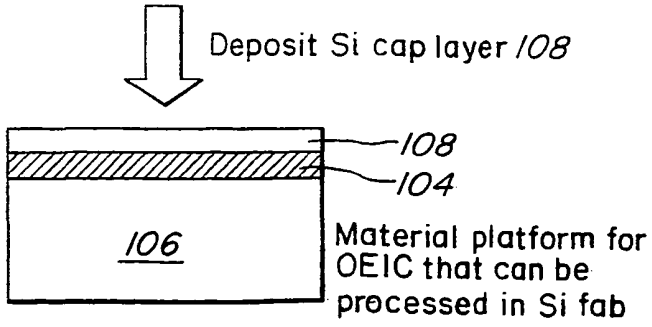


FIG. 1D

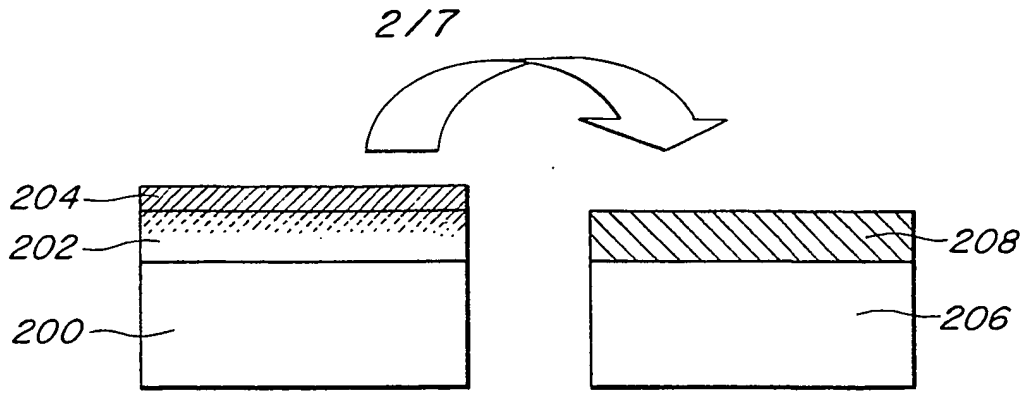


FIG. 2A

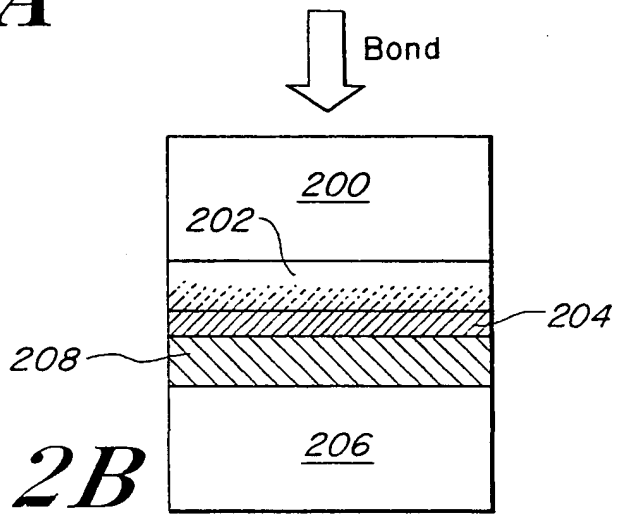


FIG. 2B

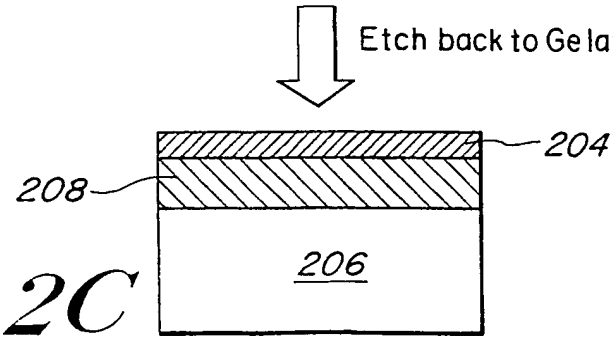


FIG. 2C

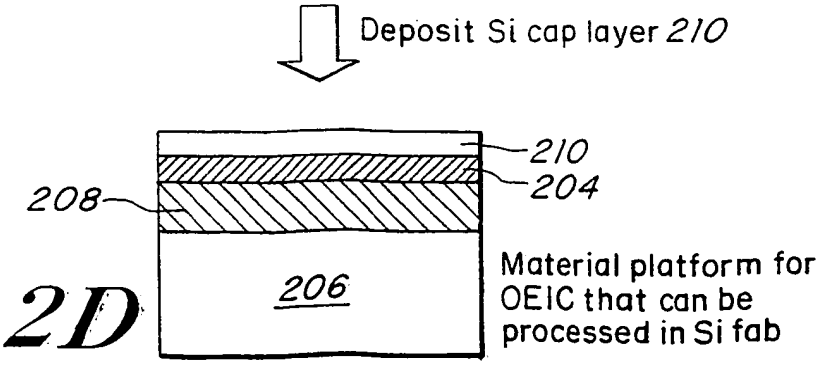


FIG. 2D

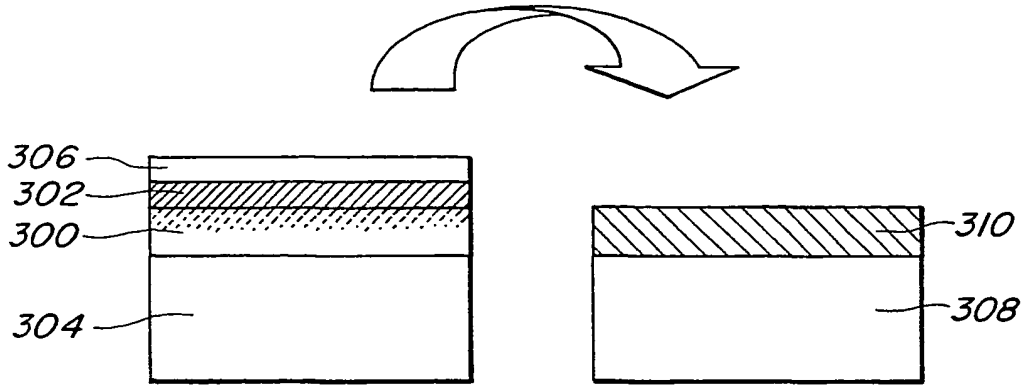


FIG. 3A

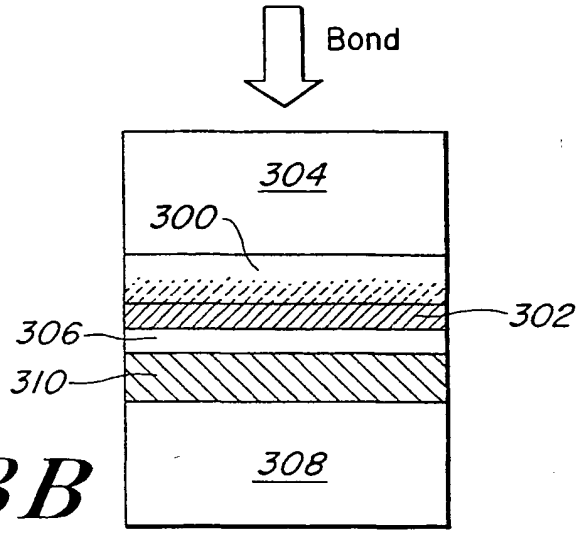


FIG. 3B

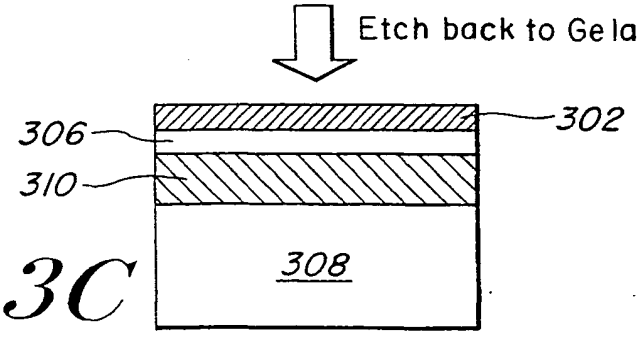


FIG. 3C

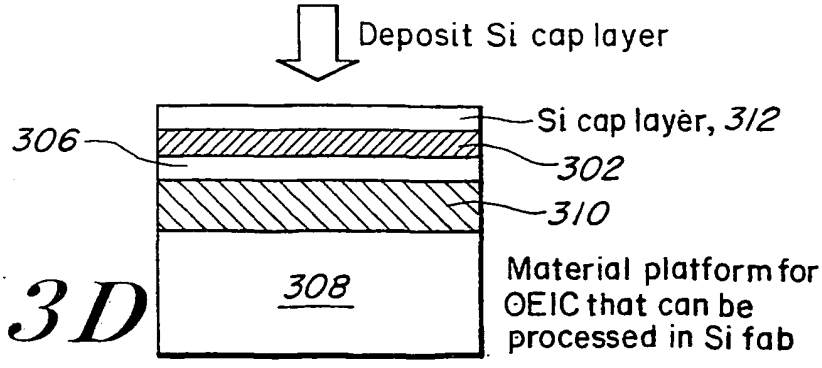


FIG. 3D

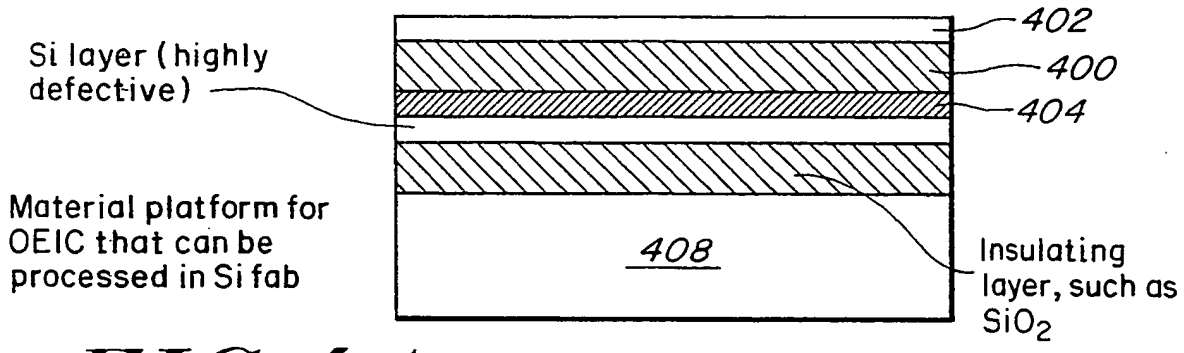
Si layer (highly defective)
Material platform for OEIC that can be processed in Si fab
402
400
404
408
Insulating layer, such as $SiO_2$

FIG. 4A

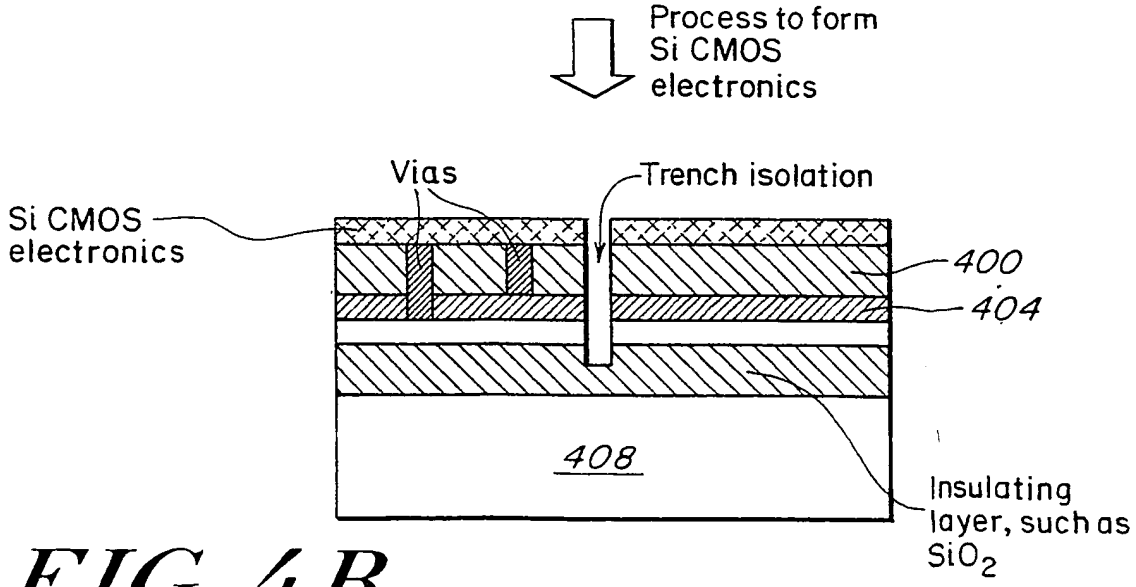
Process to form Si CMOS electronics
Vias
Trench isolation
Si CMOS electronics
400
404
408
Insulating layer, such as $SiO_2$

FIG. 4B

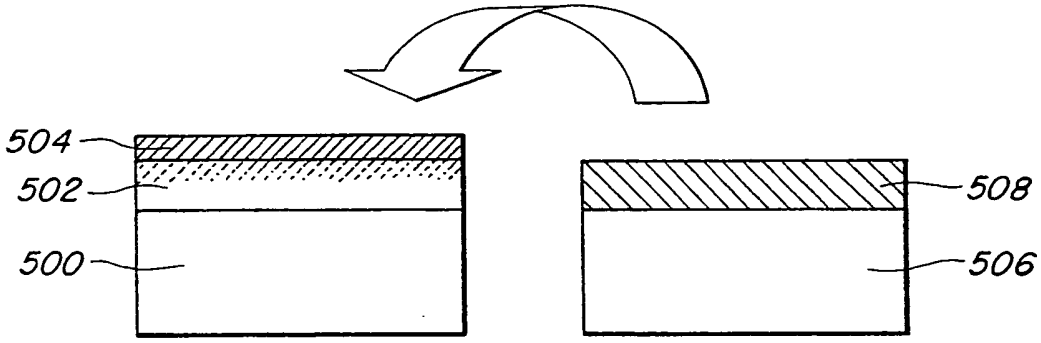


FIG. 5A

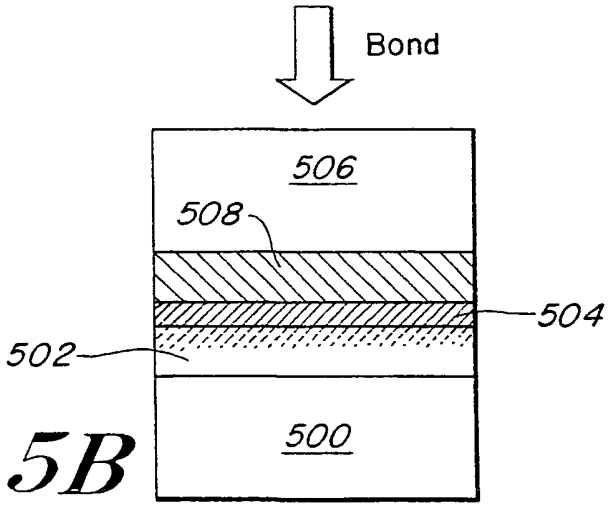


FIG. 5B

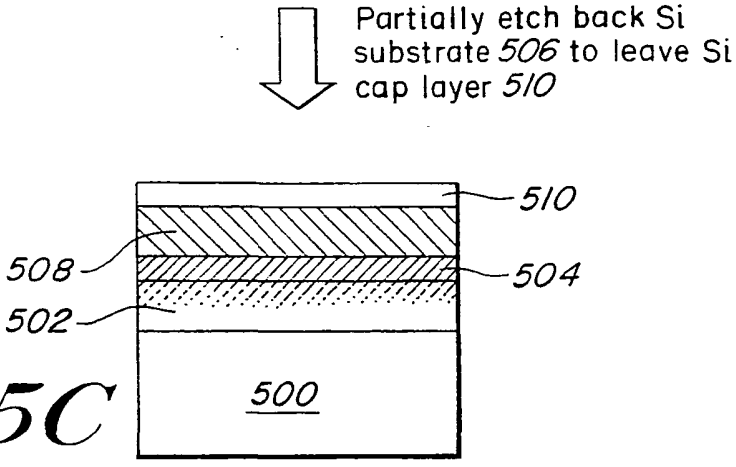


FIG. 5C

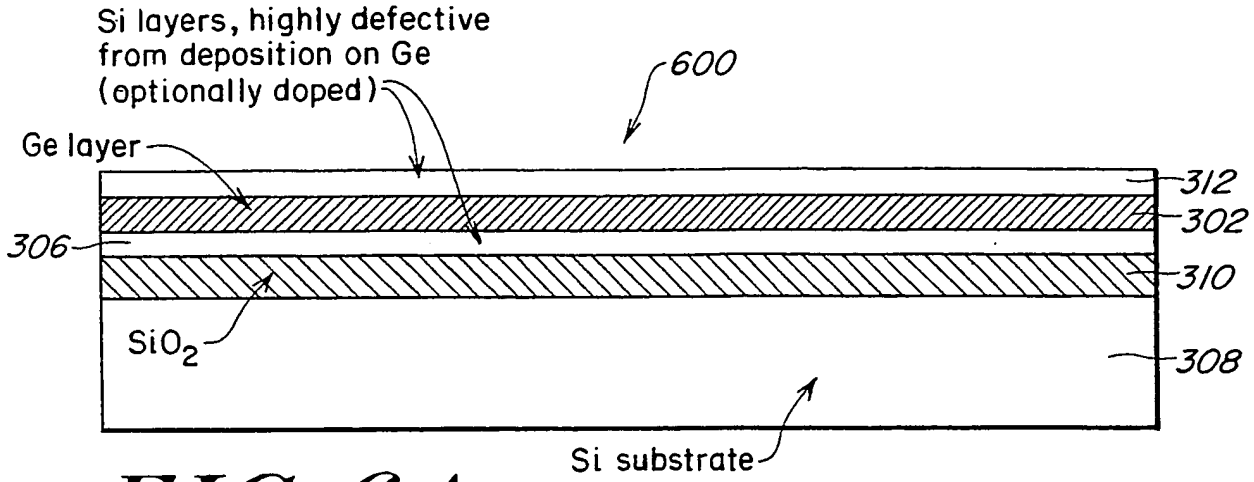


FIG. 6A

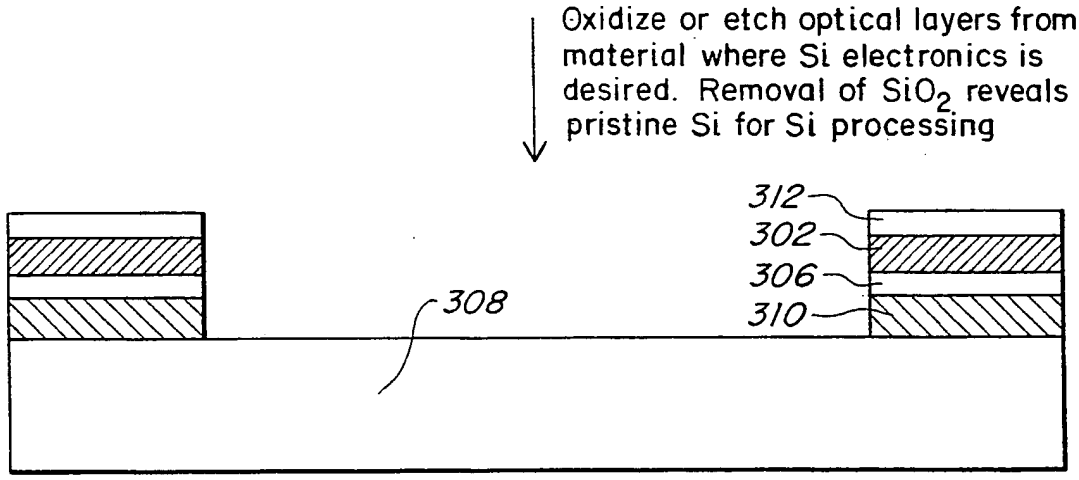


FIG. 6B

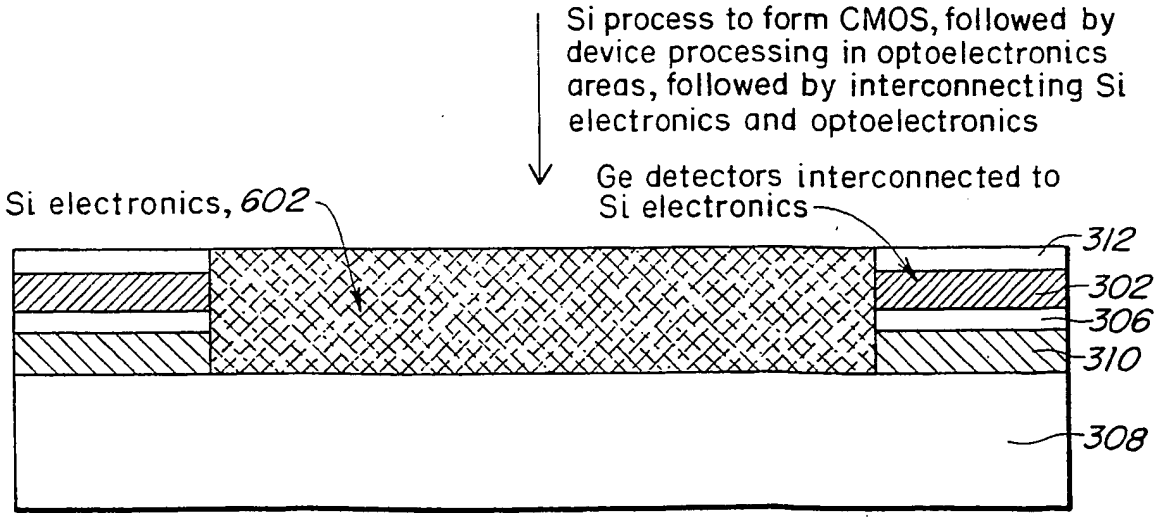


FIG. 6C

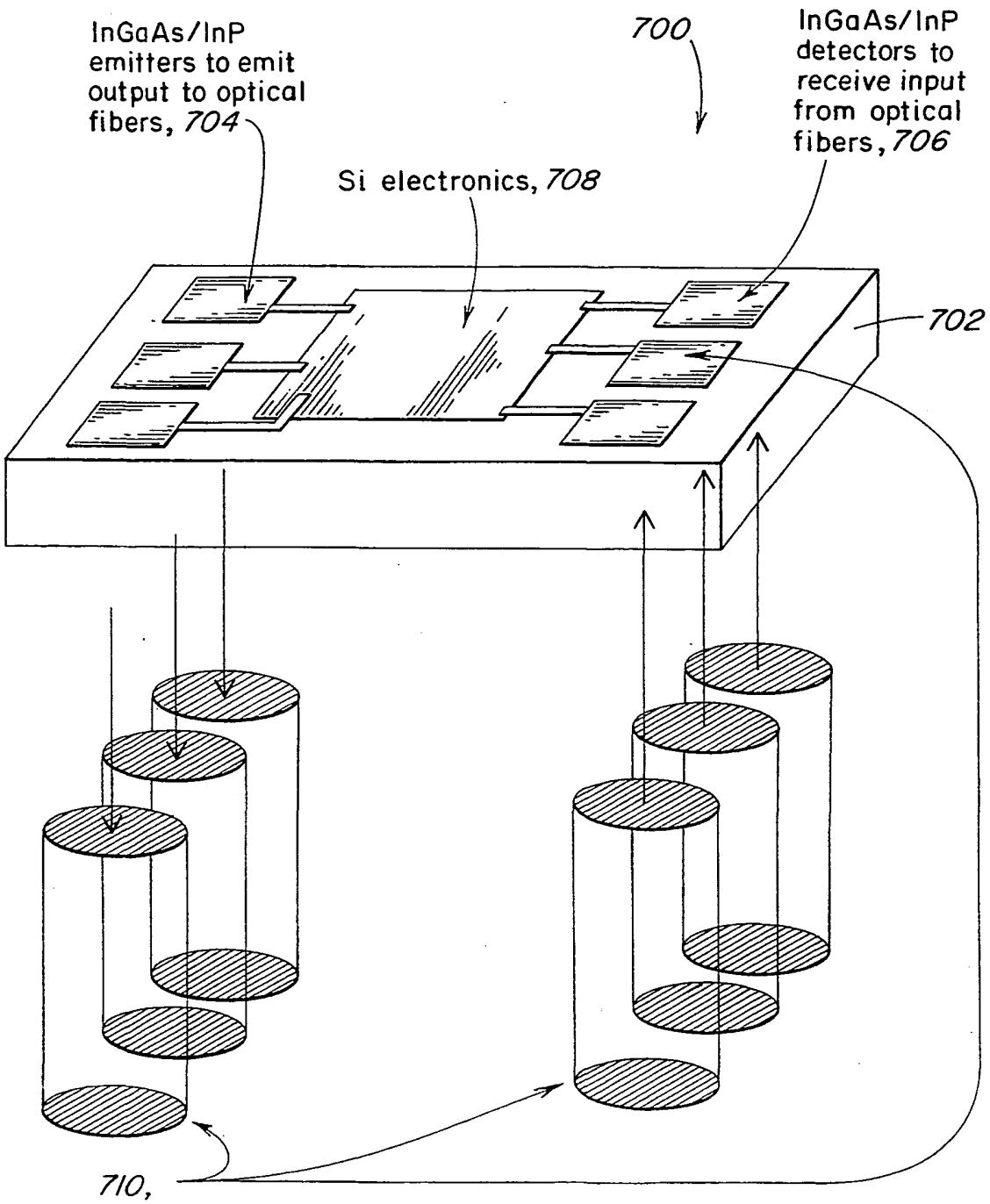
InGaAs/InP emitters to emit output to optical fibers, 704
700
InGaAs/InP detectors to receive input from optical fibers, 706
Si electronics, 708
702
710,
Butt-coupled fibers into Si substrate recesses since Si is transparent to long IR wavelengths); alternative is to have v-grooves etched in Si for edge-coupling, or a support layer with holes for top-down alignment

FIG. 7

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(72) Inventor: **FITZGERALD, Eugene, A.**; 7 Camelot Road, Windham, NH 03087 (US).

(74) Agent: **BASTIAN, Michael J.**; Tasta, Hurwitz & Thibeault, LLP, High Street Tower, 125 High Street, Boston, MA 02110 (US).

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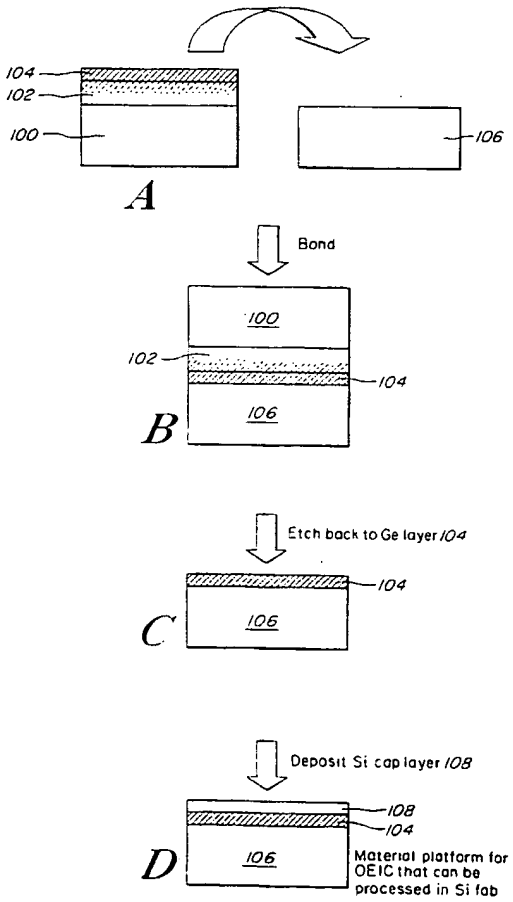
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

*[Continued on next page]*

(54) Title: SILICON WAFER WITH EMBEDDED OPTOELECTRONIC MATERIAL FOR MONOLITHIC OEIC




(57) Abstract: A structure with an optically active layer embedded in a Si wafer, such that the outermost epitaxial layer exposed to the CMOS processing equipment is always Si or another CMOS-compatible material such as $SiO_2$. Since the optoelectronic layer is completely surrounded by Si, the wafer is fully compatible with standard Si CMOS manufacturing. For wavelengths of light longer than the bandgap of Si (1.1 μm), Si is completely transparent and therefore optical signals can be transmitted between the embedded optoelectronic layer and an external waveguide using either normal incidence (through the Si substrate or top Si cap layer) or in-plane incidence (edge coupling).

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7 August 2003

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01S5/02 H01L27/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, INSPEC

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[X] Further documents are listed in the continuation of box C.

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| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Claessen, L |

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| Category ° | Citation of document, with indication,where appropriate, of the relevant passages | Relevant to claim No. |
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